INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

SYNTHESIZED SCHOOL PROGRAM

ACADEMIC UNIT: Escuela Superior de Cómputo
ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales
LEARNING UNIT: Advanced Architectures **Level:** III

AIM OF THE LEARNING UNIT:
The student creates high-performance computing components based on computer advanced architectures.

CONTENTS:

I. Parallelism
II. Pipelining and Superscalar processors
III. Vectorial and Array Computers
IV. Multiprocessor Systems

TEACHING PRINCIPLES:
This learning unit will be approached through a learning strategy based on heuristic and analogical methods, and study cases. This will lead to learning activities that will guide the development of abstraction skills, analysis, comparison, design and recreation of components in advanced architectures, using theoretical and practical tools; such as the creation and simulation of components in advanced architectures for its analysis and application on specific computer systems. The activities to be held in classroom are: collaborative and participatory work, brainstorming, documentary research, worksheets, additional presentation of topics, guided discussion, review of case studies and simulations at components of advanced architectures. Teacher takes the responsibility to decide to subjects of documentary research, review of case studies, analyzes, as well as to set the preparation and handing terms.

EVALUATION AND PASSING REQUIREMENTS:
The program will evaluate the students in a continuous formative and summative way, which will lead students into the completion of learning portfolio. Some other assessing methods will be used, such asself-assessment rubrics, peer assessment and hetero.
Other means to pass this Unit of Learning:

- Evaluation of acknowledges previously acquired, based on the issues defined by the academy.
- Official recognition by either another IPN Academic Unit of the IPN or by a national or international external academic institution besides IPN.

REFERENCES:

- Hwang, Kai (1993). "*Advanced computer architecture: parallelism, scalability, programmability".* (1ª Ed). EUA: McGraw-Hill. ISBN 9780070316225.
- Jadhav, S.S. (2009). *"Advanced Computer Architecture and Computing"*. (2a Ed). India: Technical Publications Pune. ISBN 9788184315721.
- Parhami, Bhrooz (2007). *"Arquitectura de computadoras: De los microprocesadores a las supercomputadoras".* (1ª Ed). México: McGraw Hill. ISBN 9789701061466
- Shiva, Sajjan G. (2006). *"Advanced Computer Architectures".* (1ª Ed). EUA: CRC Taylor & Francis. ISBN 9780849337581.
- Stallings, William (2010). *"Computer Organization and Architecture: Designing for Performance".* (8ª Ed). EUA: Prentice Hall. ISBN 9780136073734.

INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

ACADEMIC UNIT: Escuela Superior de Cómputo.
ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales
LATERAL OUTPUT: Analista Programador de Sistemas de Información
FORMATION AREA: Professional.
MODALITY: Presence.

LEARNING UNIT: Advanced Architectures

TYPE OF LEARNING UNIT: Theorical - Practical, Optative.
USE: August, 2011
LEVEL: III.
CREDITS: 7.5 Tepic, 4.39 SATCA

ACADEMIC AIM

This learning unit contributes to the profile of the Engineer in Computer Systems to develop skills in the designing and building hardware components for advanced and efficient processing to create solutions for specific computer issues. It also provides tools, to obtain a creative judgment, collaborative and participatory work and assertive communication.
This unit includes the units Discrete Mathematics, Computational Theory, Digital Design Fundamentals, Design of Digital Systems and Computer Architecture, as well as, ability to design hardware components in a hardware description language, abilities in documentary investigation and use of simulation tools.

AIM OF THE LEARNING UNIT:
The student creates high-performance computing components based on computer advanced architectures.

CREDITS HOURS
THEORETICAL CREDITS / WEEK: 3.0

PRACTICAL CREDITS / WEEK: 1.5

HOURS THEORETICAL / SEMESTER: 54

HOURS PRACTICAL / SEMESTER: 27

HOURS AUTONOMOUS LEARNING: 54

CREDITS HOURS / SEMESTER: 81

LEARNING UNIT DESIGNED BY: Academia de Sistemas Digitales

REVISED BY:

Dr. Flavio Arturo Sánchez Garfias
Subdirector Académico

APPROVED BY:

Ing. Apolinar Francisco Cruz Lázaro
Presidente del CTCE.

AUTHORIZED BY: Comisión de Programas Académicos del Consejo General Consultivo del IPN. 2011

Ing. Rodrigo de Jesús Serrano Domínguez
Secretario Técnico de la Comisión de Programas Académicos

THEMATIC UNIT: I **TITLE:** Parallelism

UNIT OF COMPETENCE

The student classifies parallel systems, based on computing paradigms and resources of parallelism.

No.	CONTENTS	Teacher-Led Instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
1.1 1.1.1 1.1.2 1.1.3	Computing Paradigms Serial Pipeline Parallel	0.5		1.0		5B, 2B, 1B, 3B Y 4C
1.2 1.2.1 1.2.2	Classification of parallel systems Flynn's classification Others classifications	1.0		2.0		
1.3 1.3.1 1.3.2 1.3.3	Parallelism Sources Control Parallelism Data Parallelism Flow Parallelism	1.5		2.0		
1.4 1.4.1 1.4.2 1.4.3	Parallel System Throughput Quantities and performance measures Models of *speed-up* performance Models Based on Grain Size	1.0	1.5	3.0	3.0	
	Subtotals:	4.0	1.5	8.0	3.0	

TEACHING PRINCIPLES

Framing and team-work organization.

This learning unit will be approached through a learning strategy based on heuristic and analogical methods, enabling the consolidation of the following learning techniques: worksheet, documentary research, led discussion, concept mapping, and team presentation of complementary issues and developed of a practical under a case study to evaluate the performance of a parallel system. Teacher takes the responsibility to decide to subjects of documentary research, review of case studies, analyzes and simulations performed as well as to set the preparation and handing terms.

LEARNING EVALUATION

Assessment

Portfolio of Evidences:

Worksheet	15%
Concept Map	10%
Team Presentation	15%
Report of Practical	25%
Rubric of Self-Evaluation	3%
Rubric of Co-Evaluation	2%
Evidence of Learning	30%

THEMATIC UNIT: II **TITLE:** Pipelining and superscalar processors

UNIT OF COMPETENCE

The student experiences techniques pipelining and superscalar processing, based on principles of pipelining design.

No.	CONTENTS	Teacher-Led Instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
2.1	Principles and Pipelining Implementation.	1.0	1.5	2.0	3.0	6B, 2B, 5B, 1B Y 3B
2.1.1	Linear Pipeline Processors.					
2.1.1.1	Asynchronous Model.					
2.1.1.2	Synchronous Model.					
2.2	Pipeline Processor Classification	1.0		2.0		
2.2.1	According to Level of Processing.					
2.2.2	According to Pipeline Configurations and Control Strategies					
2.3	Arithmetic Pipeline Design.	1.0		2.0		
2.3.1	Computer Arithmetic Principles.		1.5		3.0	
2.3.2	Arithmetic Pipeline Stages					
2.3.3	Multiply Pipeline Design.					
2.4	Design Aspects of Instruction Pipeline.	1.0		2.0		
2.4.1	Instruction Execution Phases.					
2.4.2	Mechanisms for Instruction Pipelining.					
2.4.3	Dynamic Instruction Scheduling.					
2.4.4	Branch Handling Techniques.					
2.5	Superscalar Processors	1.5		2.0		
2.5.1	Design Superscalar Pipelining.					
2.5.2	Design Superpipelining.					
2.5.3	Supersymmetry and design solutions.					
2.6	Case Study: Pentium Processor	0.5		2.0		
	Subtotals:	6.0	3.0	12.0	6.0	

TEACHING PRINCIPLES

This learning unit will be approached through a learning strategy based on heuristic and analogical methods, enabling the consolidation of the following learning techniques: worksheet, documentary research, led discussion, concept mapping, team presentation of complementary issues and developed of practicals, comparing trough case studies techniques Intel Pentium Processor Pipeline.

LEARNING EVALUATION

Assessment	
Portfolio of Evidences:	
Worksheet	05%
Concept Map	05%
Comparison Chart	10%
Team Presentation	05%
Report of Practical	25%
Case study report	15%
Rubric of Self-Evaluation	3%
Rubric of Co-Evaluation	2%
Evidence of Learning	30%

THEMATIC UNIT: III **TITLE:** Vector and Array Computers

UNIT OF COMPETENCE

The student verifies the efficiency of vector and array architectures based on design principles and purposes of those architectures.

No.	CONTENTS	Teacher-Led Instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
3.1	Vector Processors	1.5	1.0	3.0	2.0	5B,2B,1B,3B,6B,7C 4C
3.1.1	SIMD, MIMD, VLIW, EPIC					
3.1.2	Basic Vector Processor					
3.1.3	Interlaced or Interleaved Memory					
3.1.4	Vector length and separation of elements					
3.1.5	Relative performance between vector and scalar					
3.2	Array Processors	1.5	1.0	3.0	2.0	
3.2.1	Basic Organization					
3.2.2	Internal structure of a processing element					
3.2.3	Matrix Instructions					
3.2.4	SIMD Matrix Multiplication					
3.2.5	Associative Processors					
3.2.6	Associative Memories on Hardware		0.5		1.0	
3.3	Case Study: Intel Pentium 4, IBM Power4 and ARM11 MPCore	1.0		2.0		
	Subtotals:	4.0	2.5	8.0	5.0	

TEACHING PRINCIPLES

This learning unit will be approached through a learning strategy based on heuristic and analogical methods, enabling the consolidation of the following learning techniques: worksheet, documentary research, led discussion, concept mapping, team presentation of complementary issues and development of practicals, comparing trough case studies techniques Intel, IBM and ARM vector and array processors.

LEARNING EVALUATION

Assessment	
Portfolio of Evidences:	
Worksheet	5%
Concept Map	5%
Comparison Chart	15%
Team Presentation	5%
Report of Practical	20%
Case study report	15%
Rubric of Self-Evaluation	3%
Rubric of Co-Evaluation	2%
Evidence of Learning	30%

THEMATIC UNIT: IV **TITLE:** Multiprocessor Systems

UNIT OF COMPETENCE

The student simulates multiprocessor systems based on interconnection networks and parallel algorithms.

No.	CONTENTS	Teacher-Led Instruction HOURS		Autonomous Learning HOURS		REFERENCES KEY
		T	P	T	P	
4.1	Multiprocessor system description (features, usability and benefits).	0.5		1.0		5B, 2B, 1B y3B
4.2	Memory configurations in a multiprocessor system.	0.5		1.0		
4.2.1	Shared memory multiprocessor systems.					
4.2.2	Distributed memory multiprocessor systems.					
4.3	Interconnection networks	1.5		3.0		
4.3.1	Timeshare common channel.					
4.3.2	Bar Red Cross and multiport memory.					
4.3.3	Multistage networks.					
4.3.4	Mesh network.		0.5		1.0	
4.3.5	Hypercube network.		0.5		1.0	
4.4	Parallel algorithms for multiprocessor systems.	0.5		1.0		
4.4.1	Synchronized parallel algorithms.		0.5		1.0	
4.4.2	Asynchronous parallel algorithms.		0.5		1.0	
4.5	Case study: Multicore Intel and IBM Cell.	1.0		2.0		
	Subtotals:	4.0	2.0	8.0	4.0	

TEACHING PRINCIPLES

This unit will be addressed from the strategy of case-based learning and heuristic methods and analog, allowing the consolidation of the following learning techniques: worksheet, documentary research, led discussion, concept mapping, comparison chart, exhibition equipment complementary issues, work experience, simulations of parallel algorithms and case studies of multiprocessor systems from Intel and the IBM Cell.

LEARNING EVALUATION

Assessment	
Portfolio of Evidences:	
Worksheet	5%
Concept Map	5%
Comparison Chart	10%
Team Presentation	5%
Report of Practical	10%
Case study report	15%
Rubric of Self-Evaluation	3%
Rubric of Co-Evaluation	2%
Simulations	45%

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DIRECCIÓN DE EDUCACIÓN SUPERIOR

RECORD OF PRACTICALS

PRACTICAL No.	NAME OF THE PRACTICAL	THEMATIC UNITS	DURATION	ACCOMPLISHMENT LOCATION
1	Simulation and performance analysis of parallel algorithms.	I	4.5	Computer lab
2	VLSI module linear pipeline.	II	4.5	Digital electronics lab.
3	VLSI efficient multiplier.	II	4.5	Digital electronics lab.
4	Evaluation of polynomials in VLSI	III	3.0	Digital electronics lab.
5	Matrix multiplication in VLSI	III	3.0	Digital electronics lab.
6	Implementation of VLSI associative memories	III	1.5	Digital electronics lab.
7	Simulation of multiprocessors in a network of cross bar	IV	1.5	Computer lab
8	Multiprocessor simulation mesh	IV	1.5	Computer lab
9	Simulation of a synchronized parallel algorithm.	IV	1.5	Computer lab
10	Simulation of an asynchronous parallel algorithm.	IV	1.5	Computer lab
		TOTAL OF HOURS	27.0	

EVALUATION AND VALIDATION:

Practicals are considered a prerequisite for this learning unit credit.

Practicals contribute 25% of the grade of thematic unit I and II.
Practicals contribute 20% of the grade of thematic unit III.
Practicals contribute 10% of the grade of thematic unit IV.

Tests desk will be evaluated, the simulations and the written report of the results of experiments or simulations as appropriate.

PERÍOD	UNIT	EVALUATION TERMS
1	I, II	Continuous assessment 70% Written learning evidence 30%
2	III	Continuous assessment 70% Written learning evidence 30%
3	IV	Continuous assessment 100%
		Unit I and II 30% of the total of the final evaluation. Unit III 30% of the total of the final evaluation. Unit IV 40% of the total of the final evaluation. Other means to pass this Unit of Learning: • Official recognition by either another IPN Academic Unit of the IPN or by a national or international external academic institution besides IPN. If accredited by Special Assessment or a certificate of proficiency, this will be based on guidelines established by the academy on a previous meeting for this purpose.

KEY	B	C	REFERENCES
1	X		Hwang, Kai (1993). *"Advanced computer architecture: parallelism, scalability, programmability"*. (1ª Ed). EUA: McGraw-Hill. ISBN 9780070316225 .
2	X		Jadhav, S.S. (2009). *"Advanced Computer Architecture and Computing"*. (2a Ed). India: Technical Publications Pune. ISBN 9788184315721.
3	X		Parhami, Bhrooz (2007). *"Arquitectura de computadoras: De los microprocesadores a las supercomputadoras"*. (1ª Ed). México: McGraw Hill. ISBN 9789701061466.
4		X	Patterson, David A. and Hennessy, John L. (2008). "Computer Organization and Design: The Hardware/Software Interface. (4ª Ed). Canada: The Morgan Kaufmann. ISBN 9780123744937
5	X		Shiva, Sajjan G. (2006). *"Advanced Computer Architectures"*. (1ª Ed). EUA: CRC Taylor & Francis. ISBN 9780849337581.
6	X		Stallings, William (2010). *"Computer Organization and Architecture: Designing for Performance".* (8ª Ed). EUA: Prentice Hall. ISBN 9780136073734
7		X	Vai, M. Michael. (2000). *"VLSI design"*. (1ª Ed). EUA: CRC Press. ISBN 9780849318764

TEACHER EDUCATIONAL PROFILE PER LEARNING UNIT

INSTITUTO POLITÉCNICO NACIONAL

SECRETARÍA ACADÉMICA

DIRECCIÓN DE EDUCACIÓN SUPERIOR

1. GENERAL INFORMATION

ACADEMIC UNIT: Escuela Superior de Cómputo.

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales **LEVEL:** III

FORMATION AREA:

Institutional	Basic Scientific	Professional	Terminal and Integration
		■	

ACADEMY: Sistemas Digitales **LEARNING UNIT:** Advanced Architectures

SPECIALTY AND ACADEMIC REQUIRED LEVEL: Master Degree or Doctor in Computer Science.

1. AIM OF THE LEARNING UNIT:

The student creates high-performance computing components based on computer advanced architectures.

2. PROFESSOR EDUCATIONAL PROFILE:

KNOWLEDGE	PROFESSIONAL EXPERIENCE	ABILITIES	APTITUDES
• Sequential and combinational logic circuits. • VLSI Design. • Hardware description. • FPGA´s • Computer Architecture. • Parallel Architectures. • MEI. • English language	• One-year-experience in VSLI design. • One-year-experience in FPGA´s development. • Two-years-experience in handling groups and collaborative work. • One-year-experience as a Professor of Higher Education.	• Analysis and synthesis. • Leadership. • Decision making. • Conflict Resolution. • Group management. • Verbal fluency of ideas. • Teaching Skills.	• Responsible. • Honest. • Respectful. • Tolerant. • Assertive. • Collaborative. • Participative.

DESIGNED BY **REVISED BY** **AUTHORIZED BY**

M. en C. Edgardo Adrián Franco Martínez
Dr. Consuelo Varinia García Mendoza
M. en C. Daniel Cruz García

Dr. Flavio Arturo Sánchez Garfias
Subdirector Académico

Ing. Apolinar Francisco Cruz Lázaro
Director

Date: 2011