AIM OF THE LEARNING UNIT:
The student implements advanced digital circuits based on field programmable logic devices.

CONTENTS:
I. FPGA architectures.
II. FPGA Application Analysis.
III. FPGA Application Design.
IV. Design simulation.
V. Design Synthesis and routing
VI. Performance analysis and debugging

TEACHING PRINCIPLES:
This learning unit will be addressed from project-oriented learning strategies, deductive and inductive methods with which to carry out learning activities that will guide the development of skills of abstraction, analysis and design of efficient algorithms; using theoretical and practical tools, such is the case of the embodiment circuit using a hardware description language (HDL) that demonstrate the concepts of the unit. The activities performed in class encourage the students some techniques, such as collaborative, participative, brainstorming, graphic organizers, documentary research, presentation of complementary topics, guided discussion and practical work in laboratory

EVALUATION AND PASSING REQUIREMENTS:
The program will evaluate the students in a continuous formative and summative way, which will lead into the completion of project portfolio. Some other assessing methods will be used, such as revisions, practical’s, class participation, exercises, learning evidences and a final project.

Other means to pass this Unit of Learning:
• Evaluation of previously acquired knowledge, with base in the issues defined by the academy.
• Official recognition by either another Academic Unit of the IPN or by a national or international external academic institution besides IPN.

REFERENCES:
ACADEMIC UNIT: Escuela Superior de Cómputo.

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales.

FORMATION AREA: Professional.

MODALITY: Full-time.

LEARNING UNIT: Advanced FPGA Devices Programming.

TYPE OF LEARNING UNIT: Theoretical - Practical, Optative.


LEVEL: III.

CREDITS: 7.5 Tepic, 4.39 SATCA

ACADEMIC AIM

This learning unit contributes to the graduate profile of the Engineer in Computer Systems, to develop skills in digital systems design and computers architecture, using the application development process based on field programmable logic devices. It also develops strategic thinking, creative thinking, collaborative work and assertive communication.

This learning unit requires the knowledge acquired in the learning units Fundamentals of Digital Design, Design of Digital Systems and Computer Architecture, as well as the ability to describe an electronic circuit using a hardware description language for programming solutions on a programmable logic device (FPGA).

AIM OF THE LEARNING UNIT:

The student implements advanced digital circuits based on field programmable logic devices.

CREDITS HOURS

THEORETICAL CREDITS / WEEK: 3.0

PRACTICAL CREDITS / WEEK: 1.5

THEORETICAL HOURS / SEMESTER: 54

PRACTICAL HOURS / SEMESTER: 27

AUTONOMOUS LEARNING HOURS: 54

CREDITS HOURS / SEMESTER: 81

LEARNING UNIT DESIGNED BY: Academia de Sistemas Digitales.

REVISED BY: Dr. Flavio Arturo Sánchez Garfias.
Subdirección Académica

APPROVED BY: Ing. Apolinar Francisco Cruz Lázaro.
Presidente del CTCE

AUTHORIZED BY: Comisión de Programas Académicos del Consejo General Consultivo del IPN

Ing. Rodrigo de Jesús Serrano Domínguez
Secretario Técnico de la Comisión de Programas Académicos
**LEARNING UNIT:** Advanced FPGA Devices Programming

**THEMATIC UNIT:** I

**UNIT OF COMPETENCE**
The student analyzes the architecture of field programmable logic devices based on the type of technology used.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
<th>REFERENCES KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Programmable logic devices</td>
<td>0.5</td>
<td>2.0</td>
<td>3B</td>
</tr>
<tr>
<td>1.1.1</td>
<td>GAL devices, PAL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1.2</td>
<td>SPLD devices</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1.3</td>
<td>CPLD devices</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.1.4</td>
<td>FPGA devices</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>FPGA Architecture</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>1.2.1</td>
<td>Logical Block</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2.2</td>
<td>Routing matrix and global signals</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2.3</td>
<td>Input and output blocks</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2.4</td>
<td>FPGA memory</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Subtotals: 1.0 4.0

**TEACHING PRINCIPLES**
This unit will be addressed from the strategy of collaborative learning and inductive teaching method, allowing the consolidation of the following learning techniques: documentary research, worksheet, concept maps, team exposition in complementary subjects.

**LEARNING EVALUATION**

Diagnostic evaluation
Portfolio of evidence:

| Worksheet | 10% |
| Conceptual map | 5% |
| Teamwork | 15% |
| Self-assessment rubrics | 5% |
| Headings of co-evaluation | 5% |
| Evidence of learning | 60% |
# Advanced FPGA Devices Programming

## THEMATIC UNIT: II

### TITLE: FPGA Application Analysis

The student characterizes the steps involved in an application based on field programmable logic devices.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
<th>REFERENCES KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Workloads</td>
<td>0.5</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>2.2</td>
<td>Latency</td>
<td>0.5</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>2.3</td>
<td>Timing</td>
<td>1.0</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>2.4</td>
<td>Synthesis areas</td>
<td>1.0</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>2.5</td>
<td>Area Optimization</td>
<td>0.5</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>2.6</td>
<td>Power</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.7</td>
<td>Power optimization</td>
<td>0.5</td>
<td>2.0</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Subtotals: 2.0 3.0 8.0 2.0

## TEACHING PRINCIPLES

This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: worksheet, documentary research, directed discussion, concept mapping, problem solving, and conduct additional issues of practice.

## LEARNING EVALUATION

Diagnostic evaluation:
- Portfolio of evidence:
  - Worksheet: 5%
  - Conceptual map: 5%
  - Problems Handbook: 10%
  - Teamwork: 10%
  - Practice Reports: 20%
  - Project Implementation: 10%
  - Self-assessment rubrics: 5%
  - Headings of co-evaluation: 5%
  - Evidence of learning: 30%
**THEMATIC UNIT:** III  
**TITLE:** FPGA Application Design

**UNIT OF COMPETENCE**
The student design hardware applications based on field programmable logic devices.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
<th>REFERENCES KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>T</td>
<td>P</td>
<td>T</td>
</tr>
<tr>
<td>3.1</td>
<td>Hierarchical design</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
</tr>
<tr>
<td>3.2</td>
<td>Behavioral-level design</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
</tr>
<tr>
<td>3.3</td>
<td>Level design data flow</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
</tr>
<tr>
<td>3.4</td>
<td>Gate level design</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
</tr>
</tbody>
</table>

Subtotals: 2.0 4.0 8.0 2.0

**TEACHING PRINCIPLES**
This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: worksheet, documentary research, directed discussion, concept mapping, problem solving, teamwork and complementary topics internships.

**LEARNING EVALUATION**

Diagnostic evaluation  
Portfolio of evidence:  
Worksheet 5%  
Conceptual map 5%  
Problems Handbook 10%  
Teamwork 10%  
Practice Reports 20%  
Project Implementation 10%  
Self-assessment rubrics 5%  
Headings of co-evaluation 5%  
Evidence of learning 30%
LEARNING UNIT: Advanced FPGA Devices Programming

THEMATIC UNIT: IV

UNIT OF COMPETENCE
The student simulates the operation of applications based on field programmable logic devices.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
<th>REFERENCES KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Behavioral simulation</td>
<td>0.5</td>
<td>2.0</td>
<td>4B</td>
</tr>
<tr>
<td>4.2</td>
<td>Functional simulation</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>4.3</td>
<td>Timing simulation</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>4.4</td>
<td>Printed circuit level simulation</td>
<td>0.5</td>
<td>2.0</td>
<td></td>
</tr>
</tbody>
</table>

Subtotals: 2.0 4.0 8.0 2.0

TEACHING PRINCIPLES
This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

LEARNING EVALUATION
Diagnostic evaluation
Portfolio of evidence:
Worksheet 5%
Conceptual map 5%
Problems Handbook 10%
Teamwork 10%
Practice Reports 20%
Project Implementation 10%
Self-assessment rubrics 5%
Headings of co-evaluation 5%
Evidence of learning 30%
THEMATIC UNIT: V  
TITLE: Synthesis and routing designs

UNIT OF COMPETENCE
The student designs hardware applications based on the optimization of processes and variables involved in the stages of synthesis and routing.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Synthesis and design optimization</td>
<td>0.5</td>
<td>1.0</td>
</tr>
<tr>
<td>5.1.1</td>
<td>Logic synthesis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.1.2</td>
<td>Physical synthesis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.2</td>
<td>Partition designs with layers</td>
<td>0.5</td>
<td>1.0</td>
</tr>
<tr>
<td>5.3</td>
<td>Optimization of layers</td>
<td>0.5</td>
<td>1.0</td>
</tr>
<tr>
<td>5.4</td>
<td>Generation of constraints</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.5</td>
<td>Reducing delays in routing</td>
<td>0.5</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Subtotals: 2.0 4.0 11.0 2.0

TEACHING PRINCIPLES
This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

LEARNING EVALUATION

Diagnostic evaluation
Portfolio of evidence:
Worksheet 5%
Conceptual map 5%
Problems Handbook 10%
Teamwork 10%
Practice Reports 20%
Project Implementation 10%
Self-assessment rubrics 5%
Headings of co-evaluation 5%
Evidence of learning 30%
**THEMATIC UNIT: VI**
**TITLE:** Performance analysis and debugging

**UNIT OF COMPETENCE**
The student evaluates the operation of applications based on field programmable logic devices.

<table>
<thead>
<tr>
<th>No.</th>
<th>CONTENTS</th>
<th>Teacher led-instruction HOURS</th>
<th>Autonomous Learning HOURS</th>
<th>REFERENCES KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>Software testing</td>
<td>0.5</td>
<td>2.0</td>
<td>3B,4B</td>
</tr>
<tr>
<td>6.2</td>
<td>Hardware testing</td>
<td>0.5</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td>6.2.1</td>
<td>Test protocols and configuration</td>
<td></td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>6.2.2</td>
<td>Board-level testing</td>
<td></td>
<td>1.0</td>
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</table>

**Subtotals:**

- Teacher led-instruction: 1.0 T 2.0 P
- Autonomous Learning: 5.0 T 2.0 P

**TEACHING PRINCIPLES**
This unit will be addressed from the strategy of project-oriented learning and deductive teaching method, allowing the consolidation of the following learning techniques: brainstorming worksheet, documentary research, directed discussion, concept maps, problem solving, teamwork and conduct additional issues of practice.

**LEARNING EVALUATION**

Diagnostic evaluation
Portfolio of evidence:
- Worksheet 5%
- Conceptual map 5%
- Problems Handbook 10%
- Teamwork 10%
- Practice Reports 20%
- Project Implementation 10%
- Self-assessment rubrics 5%
- Headings of co-evaluation 5%
- Evidence of learning 30%
# RECORD OF PRACTICALS

<table>
<thead>
<tr>
<th>No.</th>
<th>NAME OF THE PRACTICAL</th>
<th>THEMATIC UNITS</th>
<th>DURATION</th>
<th>ACCOMPLISHMENT LOCATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Examples of basic designs</td>
<td>II</td>
<td>5.0</td>
<td>Digital Electronics Laboratory of the ESCOM-IPN.</td>
</tr>
<tr>
<td>2</td>
<td>Floating Point Unit</td>
<td>III</td>
<td>6.0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Asynchronous Receiver Transmitter Unit</td>
<td>IV</td>
<td>6.0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PS2-Keyboard Interface</td>
<td>V</td>
<td>6.0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PS2-Mouse interface</td>
<td>VI</td>
<td>4.0</td>
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</tr>
</tbody>
</table>

**TOTAL OF HOURS**: 27.0

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**EVALUATION AND PASSING REQUIREMENTS:**

The practicals are considered mandatory to pass this learning unit.
The practicals worth 20% in each thematic unit.
<table>
<thead>
<tr>
<th>PERIOD</th>
<th>UNIT</th>
<th>EVALUATION TERMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I y II</td>
<td>Continuous evaluation 70% and written learning evidence 30%</td>
</tr>
<tr>
<td>2</td>
<td>III y IV</td>
<td>Continuous evaluation 80% and written learning evidence 20%</td>
</tr>
<tr>
<td>3</td>
<td>V y VI</td>
<td>Continuous evaluation 90% and written learning evidence 10%</td>
</tr>
</tbody>
</table>

The learning unit I is 5% worth of the final score  
The learning unit II is 18% worth of the final score  
The learning unit III is 18% worth of the final score  
The learning unit IV is 22% worth of the final score  
The learning unit V is 27% worth of the final score  
The learning unit VI is 10% worth of the final score  

Other means to pass this Unit of Learning:  
• Evaluation of previously acquired knowledge, with base in the issues defined by the academy.  
• Official recognition by either another Academic Unit of the IPN or by a national or international external academic institution besides IPN.
<table>
<thead>
<tr>
<th>KEY</th>
<th>B</th>
<th>C</th>
<th>REFERENCES</th>
</tr>
</thead>
</table>
INSTITUTO POLITÉCNICO NACIONAL
SECRETARÍA ACADÉMICA
DIRECCIÓN DE EDUCACIÓN SUPERIOR
TEACHER EDUCATIONAL PROFILE PER LEARNING UNIT

1. GENERAL INFORMATION

ACADEMIC UNIT: Escuela Superior de Cómputo.

ACADEMIC PROGRAM: Ingeniería en Sistemas Computacionales. LEVEL III

FORMATION AREA: Institutional | Basic Scientific | Professional | Terminal and Integration


SPECIALTY AND ACADEMIC REQUIRED LEVEL: Masters Degree or Doctor in Computer Science.

2. AIM OF THE LEARNING UNIT:
The student implements advanced digital circuits based on field programmable logic devices.

3. PROFESSOR EDUCATIONAL PROFILE:

<table>
<thead>
<tr>
<th>KNOWLEDGE</th>
<th>PROFESSIONAL EXPERIENCE</th>
<th>ABILITIES</th>
<th>APTITUDES</th>
</tr>
</thead>
</table>
| • Design of Digital Systems  
• Computer Architecture  
• Microprocessors and microcontrollers  
• One or more hardware description languages  
• Knowledge of the Institutional Educational Model.  
• English Spoken. | • One year experience in the industry (preferred, not essential).  
• One year experience in courses in digital system design  
• Two year experience in managing groups and collaborative work.  
• One year experience as a Professor of Higher Education. | • Analysis and synthesis.  
• Problems resolution.  
• Cooperative.  
• Leadership.  
• Applications of Institutional Educational Model.  
• Decision making. | • Responsible.  
• Tolerant.  
• Honest.  
• Respectful.  
• Collaborative.  
• Participative.  
• Interested to learning.  
• Assertive. |

DESIGNED BY

M. en C. Miguel Ángel Vivanco
COORDINATING PROFESOR

Dr. Julio Cesar Sosa Savedra.
M. en C. Víctor Hugo García Ortega.
Dr. Mario Aldape Pérez.
COLLABORATING PROFESSORS

REVISED BY

Dr. Flavio Arturo Sánchez Garfias
Subdirector Académico

AUTHORIZED BY

Ing. Apolinar Francisco Cruz Lázaro
Director

Date: 2012